## LINEAR CIRCUITS WITH RC DEVICES

**1. OBJECTIVES**

This laboratory work has as purpose the experimental study of transmitting signals through linear circuits realized with RC elements, respectively the study of the RC high-pass filter and RC low-pass filter circuits.

**2. THEORETICAL CONSIDERATIONS**

2.1 RC high-pass circuit

The RC high-pass filter (presented in Fig. 1.1), behaves like a voltage divider, having a dividing ratio that depends on frequency, the high frequency components of a non-sinusoidal signal applied at the input appear at the output with a smaller attenuation then low frequency components. In the extreme case, at zero frequency, the capacitance reactance becomes infinite, the continuous component of the signal is not transmitted at the output, resulting the usage of the RC high-pass filter for direct current circuits separation.

### R

### C

**Ui(t)**

**Ue(t)**



## Fig.1.1

2.2 RC low-pass circuit

The RC low-pass filter (presented in Fig.1.2) behaves like a voltage divider, having a dividing ratio which depends on frequency, the low frequency components of a non-sinusoidal signal applied at the input appearing at the output with a smaller attenuation than high frequency components.

**Ui(t)**

**Ue(t)**

### C

### R



## Fig.1.2

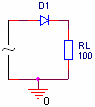
## RECTIFIERS

**1. OBJECTIVES**

This laboratory work has as purpose the experimental study of mono and double alternating rectifiers.

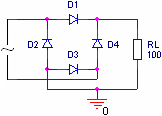
**2. THEORETICAL CONSIDERATIONS**

2.1 Mono alternating rectifier



D1 diode is on only when the anode’s voltage is positive. In this way, positive alternations are allowed and negative alternations are blocked.

2.2 Double alternating rectifier



During positive alternations D1 and D3 diodes are on and during negative alternations D2 and D4 diodes are on. In this way, at the output only positive voltage will be obtained.

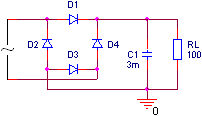
## CONTINUOUS VOLTAGE SOURCES

**1. OBJECTIVES**

This laboratory work has as purpose the experimental study of continuous voltage sources.

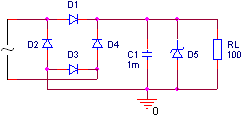
**2. THEORETICAL CONSIDERATIONS**

2.1 Filter rectifier



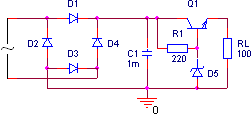
The capacitor stores energy during the time intervals in which the voltage supplied by the rectifier is greater than the voltage between the capacitor’s plates and releases energy during the time intervals in which the voltage supplied by the rectifier is lower than the voltage between the capacitor’s plates.

2.2 Parametric regulator with Zener diode



The functionality of the regulator is based on the Zener diode non-linear characteristic that allows large current variations at small reverse polarity voltages applied on the diode.

2.3 Reaction regulator with no error amplifier



Increasing vOUT voltage will determine the decrease of vBE voltage, that in turn will determine the increase of vCE and as a consequence vOUT voltage will decrease. Similar, the vOUT voltage decrease will determine the increase of vBE voltage, that in turn will determine the decrease of vCE voltage and as a consequence vOUT voltage will increase. The regulator output voltage value is vOUT=vZ-vBE.

## INVERTER WITH BIPOLAR TRANSISTOR

**1. OBJECTIVES**

This laboratory work has as purpose the experimental study of the inverter with bipolar transistor.

**2. THEORETICAL CONSIDERATIONS**

2.1 Inverter with bipolar transistor



If VIN is 0V, corresponding to 0 logic level, Q1 transistor is off and VOUT voltage will have 5V value, corresponding to 1 logical level. If VIN is 5V, corresponding to 1 logical level, Q1 transistor is on and VOUT voltage will have 0,2V value, corresponding to 0 logic level.

## TTL LOGIC CIRCUITS

**1. OBJECTIVES**

This laboratory work presents the constructive functioning characteristics of the TTL integrated circuit’s family, and the main static and dynamic parameters of this family.

**2. THEORETICAL CONSIDERATIONS**

2.1 Functioning of the circuit

**Q1**

**Q2**

**Q3**

**Q4**

**D2**

**D1**

#### D

**R2**

# **1,6K**

**R1**

# **4K**

**R4**

# **130**

**R3**

# **1K**

**VCC**

#### A

#### B

**y=AB**

**Ue**



### Fig.2.1

To show the electric functioning of the circuit in figure 2.1, let’s assume first that one of the inputs is connected to the ground (logic level "0"). As a consequence, Q1 transistor is saturated, and because of the voltage drop in it’s collector, Q2 transistor is cut-off stage. The low voltage in Q2’s emitter determines the blocking of the Q4 transistor. The Q3 transistor will be in conduction, being driven by the high potential in Q2’s collector. At the output we will obtain a high voltage, corresponding to “1” logic level.

If at both inputs we apply a voltage corresponding to “1” logic level, the basis-emitter junctions of the Q1 transistor are reversed biased and the transistor works in the reverse active stage. In this case the basis-collector of the Q1 transistor and the basis-emitter junctions of the Q2 and Q4 transistors form a chain of directly polarized diodes through the R1 resistance from the plus of the voltage source. As a consequence the Q3 and Q4 transistors will become saturated. In the same time the Q3 transistor is blocked because in it’s basis there is a smaller potential than in it’s emitter because of the voltage difference introduced by the D3 diode. Thus we obtain at the output a potential equal to Q4’s collector-emitter saturation voltage which corresponds to “0” logic level.

If we analyze the functioning of the gate from the logical point of view, we observe that it realizes the NAND function, so: 

2.2 Circuit parameters

Logical levels: VILmax = 0.8 V, VIHmin = 2 V, VOLmax = 0.4 V, VOHmin = 2.4 V and VT = 1.3V

Noise margins: ML = 0.4V and MH = 0.4V

Input and output currents: IIH = 40 μA, IIL = -1,6 mA, IOH = -800 μA and IOL = 16 mA

Fan out: FOL = 10, FOH = 20 and FO = 10

The input characteristic II=f(VI), can be obtained using the scheme in figure 2.2.



### Fig.2.5



**VIH**

**VO**

**IOL**

**150**

**400**

**VCC**

### Fig.2.3



**VIL**

**VO**

**IOH**

### 1K

### 10K

**VIH**

### Fig.2.4



**VIH**

**VO**

**VI**

### Fig.2.2

The output characteristic VOL=f(IOL) can be obtained using the scheme in figure 2.3 and the characteristic VOH=f(IOH) with the scheme in figure 2.4.

The short circuiting of the output to the ground can determine a current between 18 and 55 mA, through the Q3 transistor, if Q3, D3 and R4 work statically correct. This current is not dangerous if it has a short period. The variation of the short circuit with the supplying voltage can be observed using the scheme in figure 2.5.

In the TTL integrated circuits family there are several series of circuits, which differ one from another by the compromise between the power consumption on the gate and the propagation time, as shown in the table below:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | 74 | 74LS | 74S | 74ALS | 74AS |
| Typical static power consumption/gate [mW] | 10 | 2 | 19 | 1.2 | 8.5 |
| Typical propagation time [ns] | 10 | 9.5 | 3 | 4 | 1.5 |

The transfer characteristic of the NAND standard gate can be plotted using the layout presented in figure 2.6. The circuit formed by R1, D1-D4, connected to the gate output simulates an impedance equivalent to 10 TTL charges. The diodes are of 1N4148 type and C1 includes the output capacitances of the probes and of the connecting system.



**VI**

**VO**

**VCC**

## R1

## 400

**C1**

**15pF**

**VIH**

**D1**

**D2**

**D3**

**D4**

### Fig.2.6

The dynamic characteristics of the TTL circuits can be determined using the circuit in figure 2.7, which simulates the loading of a gate with 10 TTL charges. The rising and falling times tr and tf have the typical values 8ns and 5ns respectively. The propagation time have the following typical values: tpHL=8ns, tpLH=12ns and tp=10ns.

**VIH**

**D1**

**CS**

**15pF**

**VCC**

## R1

**D2**

**D3**

**D4**



### Fig.2.7

# TTL INTEGRATED CIRCUITS SERIES

**1. OBJECTIVES**

This work makes the comparative analysis of different TTL integrated circuits series, by presenting the fundamental gate realized by the respectively technology. There are presented the constructive-functional characteristics and the main static and dynamical parameters of each series.

**2.1 HIGH SPEED TTL SERIES**

High speed TTL series is a variant of the normal series modified in order to obtain smaller propagation times, which is to the prejudice of the power consumption. Thus, the typical propagation times for the high speed series are: tpLH = 5,9ns, tpHL = 6,2ns, and the average propagation time is tp = 6ns, so it stipulates for an improvement with over 40% more than the normal series. At the same time, the power consumption is twice bigger than that corresponding to the normal series which is: PC = 22mW.

As a structure, the fundamental TTL gate of the high speed series (figure 3.1) is very similar to that of the normal series, highlighting the following modifications. All resistors of high speed TTL gate scheme have smaller values so as the charging and discharging of internal capacities should be made faster, in order to reduce the propagation time. But these actions take place by generating greater currents, which leads to the increasing of the power consumption. High speed gate does not contain the voltage shifting diode, but a compound transistor is used in the upper output region of the complex inverter (Darlington assembly made up of the command transistor Q5 and the Q4 transistor), transistor which does not allow Q4 to enter in saturation, reducing the unblocking time of this transistor.



**Q1**

**Q2**

**Q4**

**Q3**

**D2**

**D1**

**Q5**

**R2**

# 760

**R1**

# 2,8K

**R4**

# 58

**R3**

# 470

**VCC**

### A

### B

**y=AB**

**Ue**

**R5**

# 4K

##### Fig.3.1

**2.2 LOW POWER TTL SERIES**

Low power TTL series is meant for the applications which require small power consumption. The medium power consumption for this series is reduced to PC = 1mW. The decreasing of the static power consumption was made by increasing the resistors values in the scheme, which led to the decreasing of the charging-discharging currents values. On the other hand the dynamical performances decreased, increasing the values of the propagation times. Thus, the series presents the following typical values for the propagation times: tpLH = 35ns, tpHL = 31ns, tp = 33ns.

As a construction, the scheme of the low power TTL series (figure 3.2) is identical with that of the standard TTL gate. However, the values of the resistors are increased in average with an order of magnitude.

**Q1**

**Q2**

**Q3**

**Q4**

**D2**

**D1**

### D

**R2**

# 20K

**R1**

# 40K

**R4**

# 500

**R3**

# 12K

**VCC**

### A

### B

**y=AB**

**Ue**



##### Fig.3.2

## NMOS INTEGRATED CIRCUITS

**1. OBJECTIVES**

In this laboratory work are presented the constructive functional characteristics of the family of NMOS integrated circuits and the main static and dynamic parameters of this family.

**2. THEORETICAL CONSIDERATIONS**

**2.1 The NMOS static inverter**

The layout of the NMOS static inverter is given in figure 4.1a.

**M2**

**Vo**

**CP**

**Vi**

**VDD**

**M1**



**a)**

### Fig.4.1

**c)**

**b)**

The M1 transistor is an **n** channel enhancement mode transistor and has the input characteristic in figure 4.1b, and the M2 transistor is a depletion mode transistor, having the input characteristic in figure 4.1c. This implies the threshold voltages VT of the two transistors to be different, for M1 the threshold voltage VT1 will be positive, and for M2, the threshold voltage VT2 will be negative.

The circuit presents an inverter obtained with the M1 transistor, in which M2 works as an active resistance, replacing a fixed resistance. The external load of this inverter is generally made up also of inputs of NMOS transistors, which have a very large input resistance, therefore the load has practically a character of capacitance.

In figure 4.2 are considered two cases of connecting the substrate terminals of the load transistor M2: the first case corresponding to binding the substrate terminal to the source terminal, and the second to binding the substrate terminal to a fixed potential.

**M2**

**Vo**

**Vi**

**VDD**

**M1**

**VGG**



### a)

**M2**

**Vo**

**Vi**

**VDD**

**M1**

**VGG**



**b)**

### Fig.4.2

In case the M1 transistor conducts, in order to have at the output a potential as close to zero as possible, it is necessary for the transition resistance of the load transistor M2 to be much greater then the transition resistance of the M1 transistor. To satisfy the relationship between the transition resistances of the two transistors, the dimensions of the induced channel have to be correspondingly chosen for the M1 and M2 transistors, according to the relation: .

If the inverter transistor M1 is in cut-off stage, for the case in figure 4.2a, the output voltage will be:

Vo = VGG - VT2

For VGG = VDD = 15V and VT = 4V, it follows that Vo = 11V.

In order to have at the output a potential approximately equal to VDD, the voltage applied on the gate of the M2 transistor should be increased with the value of the threshold voltage VT. In the given example VGG = VDD + VT = 19V.

If the M1 transistor is in cut-off stage, for the case in figure 4.2b, the output voltage will depend on VGG and the threshold voltage, following a relation that contains also elements (parameters) specific to the intrinsic structure of the basis substrate. For higher threshold voltages, the value of the output voltage will decrease. For this reason, in order to ensure the logical levels at the output, we try to reduce the threshold voltage through technological procedures of fabricating the MOS transistors.

**2.2 The static NAND gate**

**M3**

**Vo**

## A

**VDD**

**M2**

**VGG**

**M1**

## B



## F

### Fig.4.3

Figure 4.3 represents the static NAND gate realized with NMOS transistors. It contains two NMOS transistors, M1 and M2. On the gate of these transistors we apply the input signals; the transistors are connected in series. As a load resistance we use the M3 transistor. In order to ensure the logical levels at the output, especially a lower level of the output voltage, sufficiently close to the ground, it is necessary for the active resistance to be 20 times greater then the transition resistance of the input transistors; because of this, the series connection of many transistors is not recommended.

The following values for the logical levels are considered: VL = 0V and VH = VDD.

The functioning of the gate is the following:

* if at both inputs we apply a voltage greater then the threshold voltage VT, more precisely VIH = VDD, both M1 and M2 transistors conduct, and at the output the lower voltage level is obtained (VL ≈ 0V)
* if at least at one input a voltage smaller than VT (usually VIL=0V) is applied, the corresponding input transistor goes in cut-off stage and at the output the higher voltage level is obtained. At the output of the gate the NAND logical function is thus obtained:

F = ¬(A∙B)

**2.3 The static NOR gate**

Figure 4.4 represents a NOR gate with NMOS transistors, composed by the parallel connection of the transistors on which the logic signals are applied at input. The load resistance is realized also with a NMOS transistor.

**M3**

**Vo**

#### A

**VDD**

**M2**

**VGG**

**M1**

## B



## F

### Fig.4.4

The functioning of the gate is the following:

- if on both inputs a lower voltage than the threshold voltage VT (VIL = 0V) is applied, the transistors M1 and M2 are in cut-off stage and at the output the higher voltage level Vo = VOH = VDD is obtained.

- if at least on one input a voltage higher then the threshold voltage VT is applied, so VIH = VDD, that transistor conducts, and at the output the lower voltage level VOL ≈ 0V is obtained.

#### CMOS INTEGRATED CIRCUITS

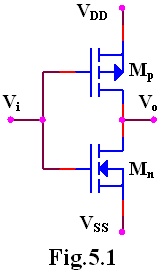
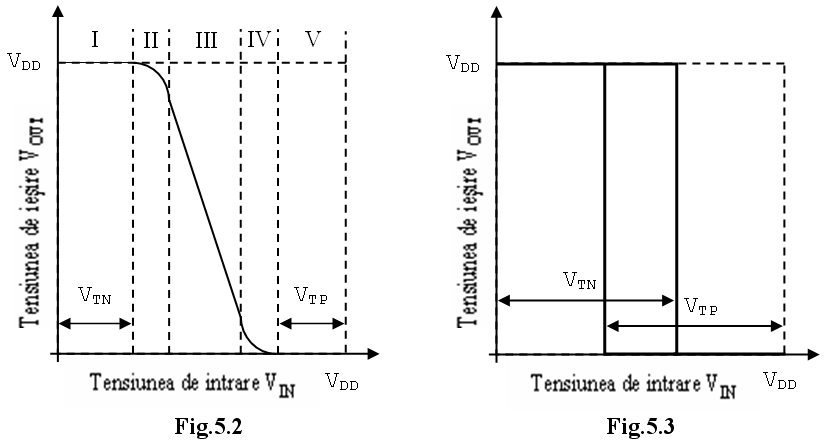
**1. OBJECTIVES**

This laboratory work intends to study the static and dynamical characteristics the CMOS integrated circuits and special features in the use of CMOS circuits.

**2. THEORETICAL CONSIDERATIONS**

2.1. CMOS Inverter

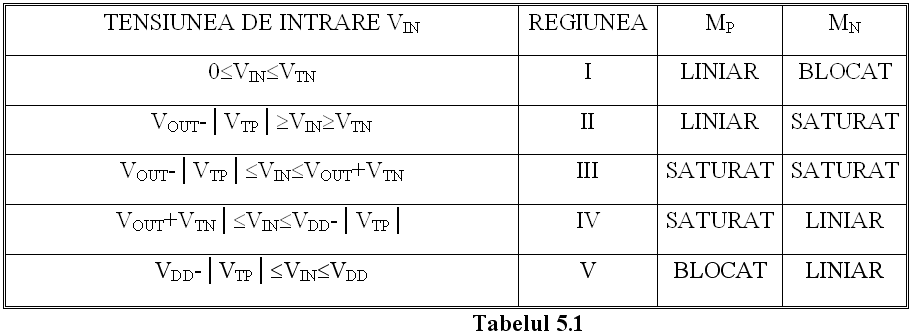
In the figure 5.1 is presented a pair of MOS transistors, one channel n and one channel p, which represents a CMOS inverter. This is the fundamental element on which logic gates are realized and any other functions needed in CMOS circuit design.



When a positive direct voltage (+VDD) representing logic “1”, is applied on common gates terminal, the NMOS transistor Mn opens and the PMOS transistor, Mp will be blocked. That ends with the output at the low voltage (VSS) source, “0” logic.

In the same way, if a low voltage is applied on the common gate, the PMOS transistor (Mp ) will be blocked and the NMOS transistor(Mn) will be opened. In this case, the output voltage will be at a high voltage (+VDD), which is logic “1”.

The transfer characteristic of the circuit is shown in the figure 5.2. This characteristic is dependent of the power supply voltage VDD. This characteristic can be divided in five distinct regions in which the functioning of the transistors Mn and Mp is presented in the table 5.1. VTN is the threshold voltage of the NMOS transistor (Mn), and VTP the threshold voltage of the PMOS transistor (Mp).



If the supply voltage VDD is smaller than VDDmin=VTN+│VTP│, the inverter will present a transfer characteristic with hysteresis, as shown in the figure 5.3 and the circuit cannot be used as a logic gate.

The typical value of threshold voltage on standard CMOS structures is:



hence VDDmin=3V, the minimal value of supply voltage for CMOS.

Input and output logic levels:

- V0Hmin=VDD-0.5V (typical value: VDD - 0.01V)

- V0Lmax=0.05V (typical: 0.01V)

- VIHmin=70%VDD

- VILmax=30%VDD

Noise margins:

MZL = VILmax - VOLmax=30%VDD

MZH = VIHmin - VOHmin=30%VDD

In use, the noise immunity is about 45.50% of the supply voltage.

#### CMOS TRANSMISSION GATE

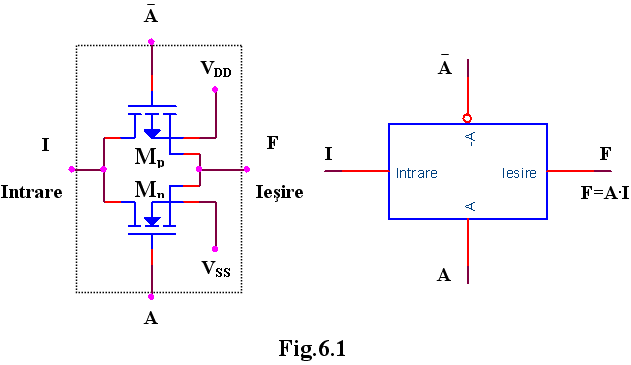
**1. OBJECTIVES**

This laboratory work intends to study the static and dynamical characteristics the CMOS integrated circuits and special features in the use of CMOS circuits.

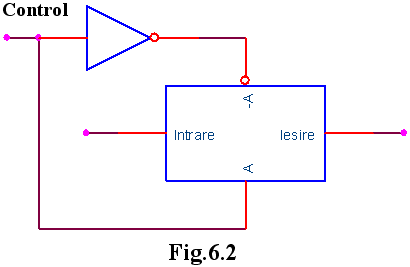
**2. THEORETICAL CONSIDERATIONS**

2.1 Transmission gate

Another fundamental element in the CMOS construction is the transmission gate. It consists from a pair of complementary MOS transistor connected in parallel, like in the figure 6.1. The circuit acts like a switch, the logic variable A being the control input. When the control input A is in logic “1” and Ā in logic “0” the transmission gate is open, and between the input and output appears a small resistance which lets the current flow in any direction. The value of the input voltage must be positive related to VSS and negative related to VDD. When A is in logic “0” and Ā is in logic “1”, the transmission gate is blocked, and there is a big resistance between the input and the output of the circuit.



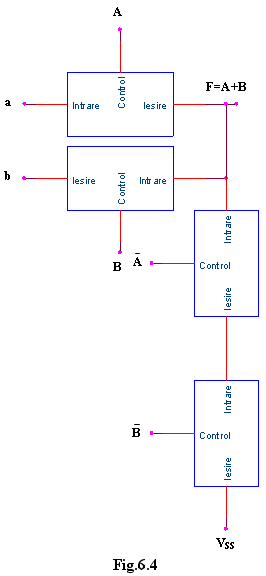
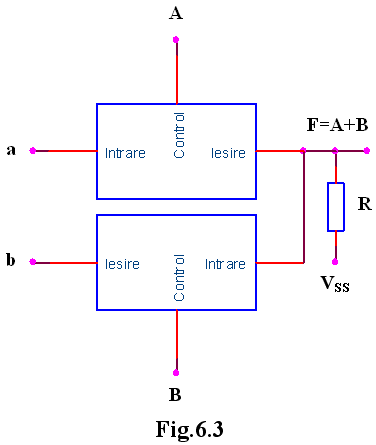
The transmission gate with an inverter forms a bilateral switch (figure 6.2).



Using transfer gates we can implement logic circuits. For example, if a=1 and b=1 the circuit from the figure 6.3 is actually an OR function. The resistance implies a power consumption in static regime if at least one gate is open.

The OR gate can be realized without resistance if there are accessible at the input the additional command signals (6.4).

**3. PRACTICAL APPROACH**



1. Study the behavior of the transmission gates as bilateral switches for the transmission of the digital signals.
2. Realize the OR logic circuits with transmission gates and verify their OR function in static and dynamic regime.

**4. THE CONTENT OF THE REPORT**

* 1. Schemes of the circuits and their functioning.
  2. Graphics obtained from the study of the static and dynamic regime of the circuits.

# **OPEN COLLECTOR LOGICAL CIRCUITS**

**1. OBJECTIVES**

There will be studied open collector logical circuits and bus designing possibilities using wired function will be analyzed.

**2. THEORETICAL CONSIDERATIONS**

To connect in parallel several gates, open collector circuits or three state circuits are used.

In the electrical scheme of the open collector TTL gates the input level and the level separator used in the creation of the fundamental gate are not be changed. However, the output level has been modified, keeping only the Q4 transistor (figure 7.1). In this case the collectors of the Q4 transistors belonging to different circuits can be connected, the junction being connected through a resistance to the supply.

**R1**

# **4K**

**R2**

# **1,6K**

**RC**

# **extern**

**D2**

**D1**

### A

### B

**Q1**

**Q2**

**Q4**

**R3**

# **1K**

**y=AB**

**Ue**

**VCC**



## Fig.7.1

The common resistance is not included in the integrated structure and it’s calculated by the scheme’s designer depending on the number of the gates connected together (n) and the number of the TTL gates that must be controlled by this common output (N).

The resistance Rc is calculated depending on the logical level of the common output, on the current generated by parallel connected gates and on the currents absorbed by the controlled gates.

In the case of 1 logical level at the output the result will be:

## Fig.7.2

#### A

#### B

#### C

#### D

#### E

#### F

**f**



**a)**

#### A

#### B

#### C

#### D

#### E

#### F

**VCC**

**f**

**RC**



**b)**

**c)**

**VI1**

**VI2**

**VO2**

**VO1**

**VCC**

**f**

**RC**





and for 0 logical level the result will be:



The values of the charge resistances are calculated as following:Vcc=5V±5%, IOH=250μA, IOL=16mA, IIL=1.6mA, IIH=40μA, VOHmin=2.4V, VOLmax=0.4V.

To create, for example, the function implemented in figure 7.2 a three level logic is necessary, leading to a great delay. The same function can be implemented with open collector circuits. The function is denoted wired-AND.



The circuit implements the AND function between the outputs of the NAND gates. The whole circuit implements the NOT-AND-OR for the group of variables at the input of the NAND gates.

The open-collector and three-state circuits are widely used for bus manufacturing. A circuit connected to a bus works, normally, both as an emitter and a receiver. For this reason, the command inputs have to allow both read and write operations from and on the bus. The word is introduced on the bus using when the RD command signal authorizes the operation. Through a WR command the word is fetched from the bus (figure 7.3.a). If only TTL circuits are connected to the bus, bus-terminators can be used (a group of resistances connected at the bus terminals to adapt against reflections) figure 7.3.b.



**VCC**

#### WT

#### RD

**linie**

**magistrală**

**a)**



**VCC**

## 180Ω

**linie de date**

**impedanţă 120Ω**

## 390Ω

**b)**

## Fig.7.3

**3. PRACTICAL APPROACH**

1. The study of the open-collector gate (figure. 7.1) functioning using the circuit from figure 72.c. For a 1 logical state at the output increase Rc until VOH decreases under 2.4V. Denote it by Rcmax and compare it with the computed one. For 0 logical at the output decrease Rc until VOL is greater than 0.4V, denote it by Rcmin and compare it with the computed one. Repeat these operations for various charges.
2. Verify the truth table of the logical function realized by the circuit in the figure 7.2.b. Study the behavior of the circuit in dynamical regime by applying at the input a rectangular signal. Observe the behavior of the circuit when a capacitance of 2000pF is connected to the output.
3. Se realizează circuitul din figura 7.3a şi se analizează comportarea în regim static şi dinamic. Implement the circuit in the figure 7.3a and analyze its dynamical and statical behavior.

**4. THE CONTENT OF THE REPORT**

* 1. Brief description of the open-collector circuits.
  2. Draw the circuits, the data tables and the graphical representations of the studied characteristics.
  3. Draw the charts obtained from the dynamical behavior of the circuits.
  4. Remarks related to the difference between the theoretical computed values and the simulated values.

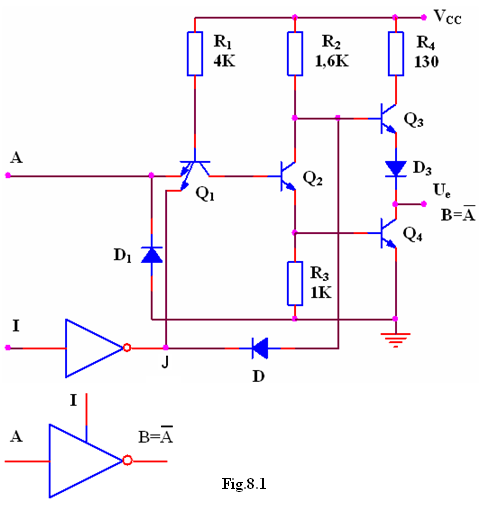
# BUS DESIGN USING THREE STATE CIRCUITS

**1. OBJECTIVES**

Three state logical circuits will be studied and there will be analyzed the designing possibilities of the buses using this type of circuit.

**2. THEORETICAL CONSIDERATIONS**

The impediments introduced by the external resistance necessary for open colector circuits are eliminated in the case of three state circuits (TSL - Three State Logic). In the output circuit of a TTL gate always one of the Q3 or Q4 transistors is on. If both transistors are off the output circuit is isolated and, seen from outside, the TTL gate presents an high impedance. Circuit has three states: 0 logical state, 1 logical state and high impedance, that leaves the output floating when both transistors are off.



The layout of an TTL inverter with three states is presented in figure 8.1.

Inhibit input I allows for ordinary NOT gate behavior if I=0. If I=1, J=0, D is on, Q1 is saturated, Q2 and Q4 are off, Q3 is off because through opened D diode its basis potential decreases to 0.7V so the circuit will present at the output an high impedance (HZ).

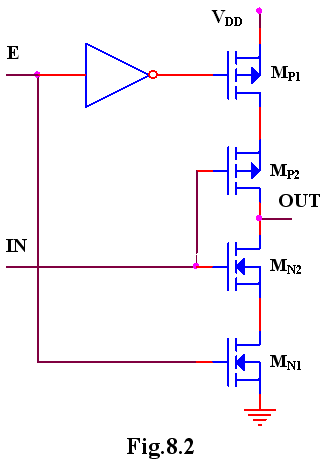
In dynamic stage, beside the known propagation times tPLH şi tPHL the following parameters appear:

- the time for high impedance establishment starting from 0 logical state tLZ, and from 1 logical state respectively, tHZ;

- the time for exiting from high impedance state and going to 0 logical state, tZL, and going to 1 logical state respectively, tZH.

Considering these delays the total propagation time through these gates is around 25 ns. This value is larger than the one for usual TTL gates but is much smaller than the value for open collector circuits.

Also, in the case of CMOS gates output circuits that can have high impedance state are available. Such a circuit contains two n channel transistors and two p channel transistors (figure 8.2). A pair of p-n transistors operates with standard NOT function, and the second pair works as on-off switch driven by the enable input E.



If E input is in 1 logical state, MN1 and MP1 transistors are on and the output can present 1 and 0 logical levels. When E input is in 1 logical state, the output impedance is high (higher than 1010Ω at 25°C).

The open-collector and three-state circuits are widely used for bus manufacturing. A circuit connected to a bus works, normally, both as an emitter and a receiver. For this reason, the command inputs have to allow both read and write operations from and on the bus. The word is introduced on the bus using when the RD command signal authorizes the operation. Through a WR command the word is fetched from the bus (figure 8.3.a). If only TTL circuits are connected to the bus, bus-terminators can be used (a group of resistances connected at the bus terminals to adapt against reflections) figure 8.3.b.

